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10/790,650	03/01/2004	Harinath B. Kamepalli	SUN040292	9771

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EXAMINER	
DINH, PAUL	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 10/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/790,650	KAMEPALLI ET AL.	
	Examiner	Art Unit	
	Paul Dinh	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Paul Dinh

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This FINAL OFFICE ACTION is a response to the amendment filed on 10/20/05.

Claims 1-11 and newly added claim 21 are pending.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Claim 5 recites first and second RTL models; claims 9-10 recites "a symbolic simulator"; therefore, these features must be clearly shown/labeled in the drawings or these features canceled from the claims.

NO NEW MATTER SHOULD BE ENTERED.

Claim Objections

Claim 1 is objected to because "the scannable state element contents" lacks antecedent basis.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form The basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1, 4-5, 7-8, 11 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Nozuyama (US Patent application Publication No. 2002/0176288)

(Claim 1)

A method for verifying scan chain equivalency between two representations (two representations = any two of: RTL, gate level, schematic in one or more of: fig 2-3, 8, 11-12, 14-18) of a circuit design having at least one scannable state element (flip-flops/latches/scan cells in fig 2, 8, 11-12, 15-18), at least one scan-out pin (SO in fig 2, 8, 11-12, 15-18) and at least one output pin (at least one output pin as shown in fig 2, 8, 11-12, 15-18) comprising:

For each representation of a circuit design (i.e., RTL, gate level, schematic in fig 2-3, 8, 11-12, 14-18), loading each scannable state element with a symbolic expression that characterizes a logical location (i.e., by one or more of control logic, test pattern, logic simulation in fig 3, 14) of said scannable element in the circuit design; and

For each representation of the circuit design (i.e., RTL, gate level, schematic in fig 2-3, 8, 11-12, 14-18), performing a scan shift operation (fig 1-2, 7-8, 11-12) to verify the scannable state element contents at said scan-out pin and said output pin of the design.

(Claim 21)

A method for verifying scan chain equivalency between two representations (see fig 2-3, 8, 11-12, 14-18, two representations = any two of: RTL, gate level, schematic) of a circuit design having at least one scannable state element (flip-flops/latches/scan cells in fig 2, 8, 11-12, 15-18), at least one scan-out pin (SO in fig 2, 8, 11-12, 15-18) and at least one output pin (at least one output pin as shown in fig 2, 8, 11-12, 15-18), comprising:

For each representation of a circuit design (i.e., RTL, gate level, schematic in fig 2-3, 8, 11-12, 14-18), loading each scannable state element with a symbolic expression that characterizes a logical location (i.e., by one or more of control logic, test pattern, logic simulation in fig 3, 14) of said scannable element in the circuit design;

For each representation of a circuit design, performing a scan shift operation (fig 1-2, 7-8, 11-12) to generate scan-out pin values at said scan-out pin; and

Comparing scan-out pin values from each representation of the circuit design to verify scan chain equivalency between two representations of the circuit design (by elements S18 and 54 in fig 3,

(Claims 4-5) Wherein the two representations of a circuit design comprise RTL and schematic model of a memory circuit (fig 3, 14, 17); first and second RTL model of a storage circuit (fig 3, 14, 17).

(Claims 7-8) wherein said loading of each scannable state element with a symbolic expression comprises simulating (simulation in fig 3, 14) said circuit design in a functional mode for a first minimum threshold number of cycles (para 0028, 0079, 0138) by applying symbolic

expressions to at least a first input (i.e., Normal input(s), SI input in fig 11-12, 15-16, 17-18)) for said circuit design, wherein said first minimum threshold number comprises a maximum sequential depth of all scannable state-elements (i.e.; number of Flip-flops (para 0079, 0158) on all paths from all primary inputs in said circuit design.

(Claim 11) wherein said scan shift operation simulating a sequence of scan clocks equal to a multiple of the number of scannable state-elements in the circuit design (para. 0110, 0159).

2. Claims 1, 4-5, 7-8, 11 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Wang et al (US Patent application Publication No. 2003/0023941)

(Claim 1)

A method for verifying scan chain equivalency between two representations (two of: RTL, HDL, schematic, and gate level description in one or more of: fig 2, 8-11, 16-17, 23, para 0003, 0006-0009, **0043; 0123**) of a circuit design having at least one scannable state element (flip-flops/latches/scan cells in fig 1, 8-12, 14-17, 19), at least one scan-out pin (one of: SCAN OUTPUT pins, SCAN OUT PORTS, SCAN-OUT SO in fig 1B, 19, 25-26) and at least one output pin (at least one output pin as shown in fig 1, 25-26) comprising:

For each representation of a circuit design (i.e., RTL, HDL, schematic, and gate level description in one or more of: fig 2, 8-11, 16-17, 23, para 0003, 0006-0009, 0043, 0123), loading each scannable state element with a symbolic expression that characterizes a logical location (i.e., by one or more of scan logic addition; Scan Constraints, Test benches, codes, logic synthesis; Pattern Generator in fig 2, 23, 25; para 0005; 0007, 0012-0013; 0032; 0036, 0046, 0104-0105, 0119) of said scannable element in the circuit design; and

For each representation of the circuit design (i.e., RTL, HDL, schematic, and gate level description in one or more of: fig 2, 8-11, 16-17, 23, para 0003, 0006-0009, 0043, 0123), performing a scan shift operation (para 0083-0084) to verify the scannable state element contents at said scan-out pin and said output pin of the design.

(Claim 21)

A method for verifying scan chain equivalency between two representations (two of: RTL, HDL, schematic, and gate level description in one or more of: fig 2, 8-11, 16-17, 23, para

0003, 0006-0009, **0043; 0123**) of a circuit design having at least one scannable state element (flip-flops/latches/scan cells in fig 1, 8-12, 14-17, 19), at least one scan-out pin (one of: SCAN OUTPUT pins, SCAN OUT PORTS, SCAN-OUT SO in fig 1B, 19, 25-26) and at least one output pin (at least one output pin as shown in fig 1, 2, 8, 11-12, 15-18) comprising:

For each representation of a circuit design (i.e., RTL, HDL, schematic, and gate level description in one or more of: fig 2, 8-11, 16-17, 23, para 0003, 0006-0009, 0043, 0123), loading each scannable state element with a symbolic expression that characterizes a logical location (i.e., by one or more of scan logic addition; Scan Constraints, Test benches, codes, logic synthesis; Pattern Generator in fig 2, 23, 25; para 0005; 0007, 0012-0013; 0032; 0036, 0046, 0104-0105, 0119) of said scannable element in the circuit design;

For each representation of a circuit design (i.e., RTL, HDL, schematic, and gate level description in one or more of: fig 2, 8-11, 16-17, 23, para 0003, 0006-0009, 0043, 0123), performing a scan shift operation (para 0083-0084) to generate scan-out pin values at said scan-out pin; and

Comparing scan-out pin values from each representation of the circuit design to verify scan chain equivalency between two representations of the circuit design (fig 25)

(Claims 4-5) Wherein the two representations of a circuit design comprise RTL and schematic model of a memory circuit (fig 8-11, 13, 16-17, 20-21); first and second RTL model of a storage circuit (fig 2 or fig 11, 13, 15-17, 20-21).

(Claims 7-8) wherein said loading of each scannable state element with a symbolic expression comprises simulating said circuit design in a functional mode for a first minimum threshold number of cycles (Para 0058, 0093) by applying symbolic expressions to at least a first input (i.e., Scan Inputs or Primary inputs in fig 1B) for said circuit design, wherein said first minimum threshold number comprises a maximum sequential depth of all scannable state-elements (para 0028) on all paths from all primary inputs in said circuit design.

(Claim 11) wherein said scan shift operation simulating a sequence of scan clocks equal to a multiple of the number of scannable state-elements in the circuit design (one or more of para 0021, 0024, 0058, 0093, 0162)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a), which forms the basis for all obviousness rejections, set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-3, 6 and 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nozuyama (US Patent application Publication No. 2002/0176288) or Wang et al (US Patent application Publication No. 2003/0023941) in view of Zhong et al (US Patent application Publication No. 2004/0015800)

Nozuyama discloses substantially all the elements in claims 2-3, 6 and 9-10 including RTL netlist, gate level description and behavior level description (fig 3, 14, para 0097) except switch level netlist, transistor level netlist; SPICE level netlist, and symbolic simulator.

Wang discloses substantially all the elements in claims 2-3, 6 and 9-10 including RTL netlist, gate level description and behavior level description (fig 2, para 0003, 0006-0009) except switch level netlist, transistor level netlist; SPICE level netlist, and symbolic simulator.

Zhong discloses the switch level netlist, transistor level netlist; SPICE level netlist, and symbolic simulator in para. 0026, 0045, 0024-0025.

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize symbolic simulator to obtain complete coverage because by using symbolic simulation, in one simulation run, many combinations of binary simulation runs are achieved to verify the design, such that the simulator verifies the complete behavior of a design in a more efficient manner than traditional simulation (Zhong para 0026) and the simulator accepts Verilog behavior, RTL, gate and transistor level inputs and works with most standard PLI routines (Zhong para 0045); and SPICE netlist is converted to a Verilog switch level netlist (Zhong para 0045). In such a case, the symbolic simulator runs symbolic simulation on the transistor level netlist and compares the results with and RTL description. Thus, if using self-

checking or reference models in Verilog, there is very little change required to use symbolic simulation (Zhong para 0045).

(Additional motivation/advantage; see para 0024-0025)

Command may be used to indicate to the simulator that an object in a HDL used to indicate a signal (e.g., a Verilog object) is to be a symbol to the simulator, such that variable assigned objects are designated as symbolic variable objects. In this manner, the existing HDLs are able to support the specification of symbolic input. Upon encountering such a programming statement, the symbolic simulator propagates logic expressions, instead of binary values, capturing the relationship from input to output.

The present invention permits a check to be inserted to perform a complete test and generate information allowing the re-creation of any identified fault. In one embodiment, the simulator is instructed to perform the check through the use of one or more programming statements that generate a File of one or more vectors (e.g., binary vectors) that may be used to locate any identified fault, thereby simplifying debug. Once an error has been identified, well-known simulators that employ binary numbers may be used to isolate the fault.

Applicant's arguments with respect to claim 1-11, and 21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is 571-272-1890. The examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Dinh
Patent Examiner